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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/960,023 | 09/21/2001 | Patrick J. Meaney | POU920010094US1 | 7005 |

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| EXAMINER |
|---|
| CHANG, ERIC |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2116 | |

DATE MAILED: 08/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | Application No. | Applicant(s) |
|---|---|---|---|
| **Office Action Summary** | | 09/960,023 | MEANEY ET AL. |
| | | Examiner | Art Unit |
| | | Eric Chang | 2116 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)☒ Responsive to communication(s) filed on <u>21 September 2001</u>.

2a)☐ This action is **FINAL**.     2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

4)☒ Claim(s) <u>1-13</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-13</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

## Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>21 September 2001</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

## DETAILED ACTION

1.      Claims 1-13 are pending.

### *Claim Objections*

2.      The applicant or their representatives are urged to review the specification and submit

corrections for all mistakes of a grammatical, clerical, or typographical nature.  **For example,**

please change the following:

3.      Claim 7 is objected to because of the following informalities:  the term "claibration" on

line 4 of the claim should read, "calibration".  Appropriate correction is required.

4.      Claim 8 is objected to because of the following informalities:  the term "mannter" on line

3 of the claim should read, "manner".  Appropriate correction is required.

5.      Claim 10 is objected to because of the following informalities:  the term "whrein" on line

1 of the claim should read, "wherein".  Appropriate correction is required.

6.      Claim 11 is objected to because of the following informalities:  the term "shifing" on line

4 of the claim should read, "shifting".  In addition, the term "intrface" on line 5 of the claim

should read, "interface".  Appropriate correction is required.

7.      Claim 13 is objected to because of the following informalities:  the term "stae" on line 8

of the claim should read, "state".  Appropriate correction is required.

### *Claim Rejections - 35 USC § 103*

8.      The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains.  Patentability shall not be negatived by the
> manner in which the invention was made.

9.      Claims 1-2, 4-6, 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable

over U.S. Patent 6,198,689 to Yamazaki, in view of U.S. Patent 5,742,650 to Nuckolls et al.

10.     As to claim 1, Yamazaki discloses the method of recalibrating a source-synchronous,

self-calibrating interface in a computer system, comprising the steps of: fencing the interface

[col. 3, lines 46-48]; recalibrating the interface using clock readjustment [col. 3, lines 48-50]; and

unfencing the interface [col. 3, lines 50-52].

It would be obvious to one or ordinary skill in the art that the method taught by Yamazaki

may be applied to any other source-synchronous [col. 1, lines 17-26], self-calibrating interface

[col. 1, lines 70-10], such as may be found in an SMP computer system [col. 19, lines 37-46],

substantially as claimed. Yamazaki teaches all of the limitations of the claim, including that the

circuitry should not attempt to process data while the clocks are being recalibrated [col. 3, lines

31-37], but does not teach that the computer system is halted during the recalibration process.

Nuckolls teaches that a circuit has its operation halted [col. 3, lines 42-43] while its associated clocks are being recalibrated [col. 3, lines 48-57], and that its clocks are restarted [col. 3, lines 57-64] thereafter. Thus, Nuckolls teaches a clock recalibration process similar to that of Yamazaki.

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the processor halting means as taught by Nuckolls. One of ordinary skill in the art would have been motivated to do so that the circuit does not attempt processing while the clocks are not in a stable synchronized state.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of recalibrated clocks used by a circuit in its processing. Moreover, the processor halting means taught by Nuckolls would improve the robustness of Yamazaki because it ensures the processor does not operate while the clocks are being recalibrated by halting the processor in addition to preventing input from the interface.

11.    As to claim 2, Nuckolls discloses the halting operations are done with a system quiesce operation [col. 1, lines 16-25].

12.    As to claim 4, Yamazaki discloses calibrating the interface is accomplished by recalculating the frequency and applying the appropriate delay adjustment to the clock [col. 5, lines 50-67, and col. 6, lines 1-8].

13.    As to claim 5, Yamazaki discloses a method for re-calibration of an interface,

comprising: putting the system of the interface into a wait state [col. 3, lines 46-48]; performing

a initialization process for calibration [col. 3, lines 48-50]; taking the system of the interface out

of said wait state [col. 3, lines 50-52].


14.    As to claim 6, Yamazaki discloses a step of data deskew has been performed as part of

the original system interface initialization, without deskewing data during said fast initialization

step performed for re-calibration [col. 2, lines 11-24, and 55-58].


15.    As to claim 10, Yamazaki discloses wherein a quiesce of the system of the interface is

performed prior to performing a fast initialization process for calibration [col. 3, lines 46-48];

and during calibration, the step of calibrating the interface recalculates the frequency of the clock

for the interface and applies an appropriate delay adjustment to the clock for the interface [col. 3,

lines 48-50]; after which the system for the interface is unquiesced before commencing

operations to allow interface use again [col. 3, lines 50-52].


16.    As to claim 12, Yamazaki discloses the recalibration stem includes re-calculating the

clock frequency of the interface against the current hardware and re-applying the clock

frequency calculation to the clock delay [col. 5, lines 50-67, and col. 6, lines 1-8] when the

machine is being cycled down to failure and the major change needing re-calibration is cycle

time [col. 3, lines 53-67].

17.     Claims 3, 7-9, 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over

U.S. Patent 6,198,689 to Yamazaki, in view of U.S. Patent 5,742,650 to Nuckolls et al., and in

further view of U.S. Patent 6,470,458 to Dreps et al.

18.     As to claim 3, Yamazaki and Nuckolls teach all of the limitations of the claim, including

synchronizing an interface clock with an external reference clock, but do not teach that the

recalibration of the interface is accomplished by sampling a known data pattern.

        Dreps teaches a clock recalibration method similar to that of Yamazaki and Nuckolls.

Dreps teaches that sampling a known data pattern in order to synchronize clocks across data

interface [col. 2, lines 34-42] is well known. Dreps further teaches using a state machine to

sample data patterns to perform said synchronization.

        At the time that the invention was made, it would have been obvious to a person of

ordinary skill in the art to employ the data-sampling state machine as taught by Dreps.  One of

ordinary skill in the art would have been motivated to do so, so that data transmission across the

interface would be correctly synchronized.

        It would have been obvious to one of ordinary skill in the art to combine the teachings of

the cited references because they are both directed to the problem of synchronizing data transfer

across a data interface by aligning reference clocks.  Moreover, the data-sampling state machine

means taught by Dreps would improve the effectiveness of Yamazaki and Nuckolls by providing

an improved method and system for synchronization.

19.     As to claim 7, Dreps discloses sending a calibration pattern and allowing calibration logic

to re-center the clock applicable to the interface to compensate for new environmental conditions

and circuit changes [col. 1, lines 42-53].


20.     As to claims 8-9, Yamazaki discloses the recalibration of the interface is triggered

periodically in order to ensure that circuit or environmental characteristics over time do not

adversely affect the operation of the interface [col. 2, lines 11-24]. Yamazaki teaches that the

recalibration occurs whenever the system is turned on or comes out of a standby state. It would

be obvious to one of ordinary skill in the art that the synchronization could also be triggered by

an event, in case drift caused by environmental conditions is detected and needs to be corrected.


21.     As to claim 11, Yamazaki discloses the recalibration stem includes sending a pattern

across the interface and adjusting the clock through re-centering without data de-skewing but

with shifting to the clock to re-center the interface data capturing window for the `eye` of the

data capturing window [col. 5, lines 21-38].


22.     As to claim 13, Yamazaki discloses for quiescing the data over the interface when the

state machine enters a re-calibration state [col. 3, lines 46-48]; whereupon said a fast

initialization process for calibration is performed [col. 3, lines 48-50]; and allows data to transfer

across the interface again [col. 3, lines 50-52]. Furthermore, Dreps teaches that a state machine

controls calibration [col. 9, lines 15-31], thereby allowing the interface to restart once again.

## *Conclusion*

23.     Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Eric Chang whose telephone number is (703) 305-4612. The

examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Lynne Browne can be reached on (703) 308-1159. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ec
June 17, 2004

REHANA PERVEEN
PRIMARY EXAMINER